AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor apparatus, comprising:

a semiconductor substrate;

a metal wiring layer formed over the semiconductor substrate;

a material layer formed over the metal wiring layer and having a window therein;

a first electrode pad formed over the semiconductor substrate, and exposed through said window for providing contact between said semiconductor apparatus and external circuitry; [[and]]

a circuit formed over said semiconductor substrate and in a region under the window in the material layer exposing the first electrode pad, said circuit comprising an array of adjacent resistive elements formed of a semiconductor material, said first electrode pad being formed over said array of resistive elements such that said first electrode pad extends transversely across said array; and

at least one additional unconnected outermost resistive element adjacent to and aligned in a pattern with said resistive elements of said array.

2. (Previously Presented) The semiconductor apparatus according to Claim 1, wherein the resistive elements comprise a material selected from the group consisting of polysilicon, silicon germanium, and silicon chrome.

3. (Previously Presented) The semiconductor apparatus according to Claim 1, wherein the resistive elements include a plurality of resistors connected serially.

4. (Previously Presented) The semiconductor apparatus according to Claim 1, further comprising a MOS transistor formed over the semiconductor substrate, wherein the MOS transistor includes a gate electrode comprising a material selected from the group consisting of polysilicon, silicon germanium, and silicon chrome.

5. (Previously Presented) The semiconductor apparatus according to Claim 1, further comprising:

an insulating film formed on the semiconductor substrate in a region in a vicinity of the first electrode pad; and

a fuse element formed on the insulating film, said fuse element being in electrical contact with said plurality of resistive elements.

6. (Previously Presented) The semiconductor apparatus according to Claim 5, wherein the fuse element comprises a material selected from the group consisting of polysilicon, silicon germanium, and silicon chrome.

7. (Previously Presented) The semiconductor apparatus according to Claim 5, further comprising:

a rerouting layer formed in a region above the fuse element; and

an external connection terminal formed on the rerouting layer in a region different from a formation region of the first electrode pad.

8. (Previously Presented) The semiconductor apparatus according to Claim 5, wherein the circuit comprises a voltage setting circuit, the resistive elements comprise at least two resistors for producing a split voltage based on an input source power voltage, and the voltage setting circuit changes the split voltage according to a condition of the fuse element.

9. (Previously Presented) The semiconductor apparatus according to Claim 1, wherein the resistive elements comprise at least two resistors for producing a split voltage based on an input source power voltage, the circuit comprises a reference voltage generator for generating a reference voltage and a voltage detector including a comparator for performing a comparison of the split voltage with the reference voltage.

10. (Previously Presented) The semiconductor apparatus according to Claim 9, wherein the circuit further comprises an output driver for controlling an output voltage based on an input voltage, and the comparator of the voltage detector outputs a gate control voltage as a result of the comparison for controlling the output driver to control the output voltage.

11 – 16. (Canceled).

17. (Previously Presented) The semiconductor apparatus according to Claim 1, wherein the resistive elements include a plurality of doped semiconductor material resistors.

18. (Previously Presented) The semiconductor apparatus according to Claim 4, wherein said first gate electrode has lengthwise ends which are bent in an upward direction over an insulating film.

19. (Currently Amended) A semiconductor apparatus, comprising:

a semiconductor substrate;

an oxide film formed over the semiconductor substrate, the oxide film comprising a resistive-element formation region and a fuse-element formation region, the resistive-element formation region having a circuit comprising an array of strip-shaped resistive elements formed of a semiconductor material and at least one additional unconnected outermost resistive element adjacent to and aligned in a pattern with said resistive elements of said array;

an insulating layer formed over the oxide film and having an electrode-pad formation region, wherein the electrode-pad formation region is formed over the resistive-element formation region, and wherein the electrode-pad formation region has an electrode pad comprising a metal layer providing contact between said semiconductor apparatus and external circuitry and wherein the electrode pad extends transversely across the array of strip-shaped resistive elements; and

a passivation film formed over an uppermost metal wiring layer of the semiconductor apparatus and having a window arranged to expose the electrode pad.

20. (Previously Presented) The semiconductor apparatus of claim 19, wherein a respective low-resistance polysilicon region is formed immediately next to the lengthwise ends of each of the plurality of resistive elements.

21. (Previously Presented) The semiconductor apparatus of claim 19, wherein the oxide film further comprises a MOS transistor formation region including a MOS transistor comprising a gate electrode formed of a material comprising polysilicon, the gate electrode having lengthwise ends which are bent in an upward direction over the oxide film.

22. (Previously Presented) The semiconductor apparatus of claim 1, wherein the first electrode pad is formed on an uppermost metal wiring layer of the semiconductor apparatus, and wherein said uppermost metal wiring layer is substantially entirely covered by said material layer.

23. (Previously Presented) The semiconductor apparatus of claim 1, further comprising:

a rerouting layer including:

a second metal wiring layer formed on the material layer; and

a second electrode pad,

wherein the first electrode pad is configured to provide contact between the semiconductor apparatus and the external circuitry via the rerouting layer.

24. (Previously Presented) The semiconductor apparatus of claim 1, wherein the material layer is a passivation layer comprising one of a phosphor silicate glass film and a silicon nitride film.

25. (Previously Presented) The semiconductor apparatus of claim 1, wherein the metal wiring layer comprises a metal alloy containing silicon of approximately 1 weight percent.

26. (Previously Presented) The semiconductor apparatus of claim 25, wherein the electrode pad comprises a material substantially equivalent to a material of the metal wiring layer.